Multiple-Valued Mask-Programmable Logic Array Using One-Transistor Universal-Literal Circuits

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Abstract

This paper presents a compact multiple-valued mask-programmable logic array (MPLA) based on a MIN/TSUM (MINimum/Truncated-SUM) two-level synthesis. A universal literal in the MIN plane is decomposed into a threshold literal and a logic-value conversion (LVC) that is shared in the same column of the MIN plane. Since a threshold literal can be designed by using a single floating-gate MOS transistor, a compact MIN plane can be implemented in the proposed MPLA. Any arbitrary universal-literal circuits can be realized by programming the threshold voltage of the corresponding floating-gate MOS transistor and selecting an appropriate LVC as an input variable. The performance of the proposed MPLA is evaluated under a $0.8\mu m$ *CMOS design. It is demonstrated that its performance is superior to that of conventional PLA's.*

1. Introduction

Hardware realization of logic networks is generally time-consuming and expensive. Also, once logic functions are realized in hardware, it is difficult to change them. In some cases, one needs logic networks that are easily changeable. One such case is logic networks whose output functions need to be changed frequently, such as control logic in microprocessors. One possible method to solve the above problem is to use programmable logic arrays (PLA's)[1],[2].

On the other hand, it has been known that multiple-valued integrated circuits have attractive features which make the numbers of active devices and interconnections reduced in comparison with that of the corresponding binary ones. From this point of view, various multiple-valued PLA's have been proposed[3]-[5]. A CMOS current-mode multiple-valued PLA based on a NOR/TSUM (truncated-sum) two-level synthesis has been integrable by using a CMOS process and has consumed less silicon area of a TSUM plane by using current-mode logic circuits. However, since the number of transistors to realize a multiple-valued universal literal becomes large, it has been difficult to realize a compact NOR plane in the PLA.

This paper presents a new multiple-valued mask-programmable logic array (MPLA) based on a MIN/TSUM two-level synthesis. A universal literal in a MIN plane is represented by a threshold literal [6],[7] together with permutation of a multiple-valued input signal, called a "logic-value conversion (LVC)." Since an LVC can be shared by universal literals in the same column of a MIN plane, only the threshold literals are realized in the MIN plane.

Moreover, a threshold-literal circuit is easily designed by only a single floating-gate MOS transistor whose threshold is programmable by controlling the charge on the floating gate[8]. Consequently, a successive universal literal circuit can be designed simply.

It is demonstrated that the size of the proposed multiple-valued MPLA is one fourth of that of the conventional multiple-valued PLA in a MIN plane. The switching speed of the proposed multiple-valued MPLA is evaluated to be comparable with that of the conventional multiple-valued PLA by SPICE simulation.

2. Model of a multiple-valued PLA

In the following discussion, let the set of logic values $L = \{0, 1, \cdots, R-1\}$. Any $R-$valued $n-$variable function can be designed by using an R-valued PLA which is a MIN/TSUM two-level logic circuit. An $R-$valued $n-$variable function $f(X_1, X_2, \cdots, X_n)$ is expressed as

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the truncated sum of product terms as follows:

$$f(X_1, X_2, \cdots, X_n) = \sum_j P_j \cap [X_1^{S_{1j}} \cap \cdots \cap X_n^{S_{nj}}] \quad (1)$$

where $0 \neq P_j \in L$, $X_i \in L$, $S \subseteq L$, the symbols $\sum$ and $\cap$ stand for the truncated sum and the MIN operator, respectively, and X^S is a universal literal which is defined as[3],[4]

$$X^S = \begin{cases} R-1 & \text{if } X \in S \\ 0 & \text{otherwise.} \end{cases} \quad (2)$$

In the following description, we formulate the above universal literal using a logic-valued conversion(LVC) and a simple threshold literal. An LVC is a permutation of an input value that transforms an R-valued input value into an arbitrary R-valued output value. The LVC is a one-variable function $f(x)$ which is defined as

$$X' = f(X) = \begin{cases} p_0 & \text{if } X = 0, \\ p_1 & \text{if } X = 1, \\ \vdots & \vdots \\ p_{R-1} & \text{if } X = R-1 \end{cases} \quad (3)$$

where $X, X', p_i (0 \leq i \leq R-1) \in L$. For simplicity, the function $f(x)$ is described as

$$f = < p_0, p_1, \cdots, p_{R-1} > . \quad (4)$$

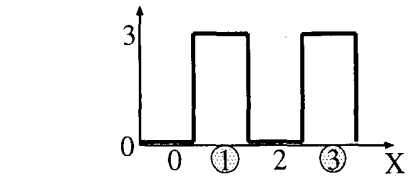
A multiple-valued threshold literal $D_Y(X)$ is an R-valued-input binary-output function which is defined as

$$z = D(X,Y) = D_Y(X) = \begin{cases} R-1 & \text{if } X \leq Y \\ 0 & \text{otherwise} \end{cases} \quad (5)$$

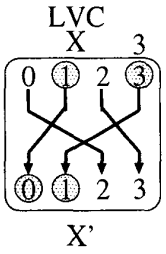
where $X, Y \in L$ and $z \in \{0, R-1\}$. Using the above definitions, any R-valued universal literal X^S is represented as

$$X^S = D_Y(X') = D_Y(f(X)). \quad (6)$$

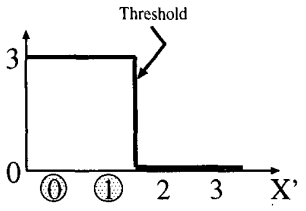
For example, in the case of $R = 4$, a universal literal $X^{\{1,3\}}$ is represented by a multiple-valued threshold literal $D_1(X')$ where the 4-valued input X is permuted to $X' = f = < 2, 0, 3, 1 >$ as shown in Fig.1.



(a) Universal literal $X^{\{1,3\}}$



(b) LVC f=<2,0,3,1>.



(c) Threshold literal $D_1(X')$

Figure 1. Realization of a universal literal.

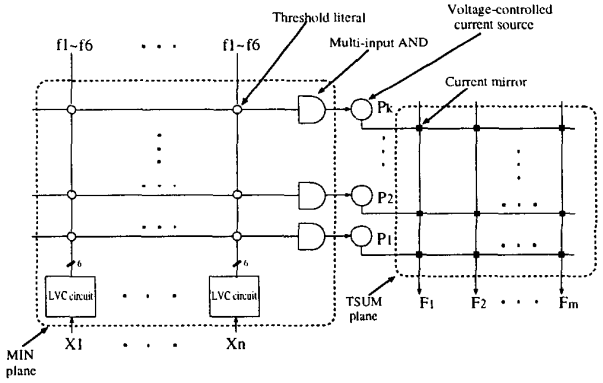


Figure 2. Structure of the proposed multiple-valued MPLA.

3. Design of a multiple-valued MPLA

The proposed multiple-valued MPLA consists of a MIN plane and a TSUM plane as shown in Fig.2. In the following discussion, we discuss about the structure of a MIN plane because the TSUM plane is the same configuration of a conventional multiple-valued PLA[3].

3.1. Multiple-valued threshold-literal circuit

A multiple-valued threshold literal whose function is described in Eq.(5) can be designed by using a single floating-gate MOS transistor. Figure 3 shows a multiple-valued threshold-literal circuit. A floating-gate MOS transistor has been used as a memory cell of multilevel flash memories[9]-[12] and it has two gates which are a control gate and a floating gate. The control-gate voltage V_x and the threshold voltage V_t in a floating gate MOS transistor, which correspond to an external input X and a stored value

Table 1. Relationship between logic values and voltage levels.

Logic value:X	0	1	2	3
Control-gate voltage:$V_x[V]$	0.0	1.7	3.3	5.0

Logic value:Y	0	1	2	3
Threshold voltage:V_t[V]	0.8	2.5	4.2	5.8

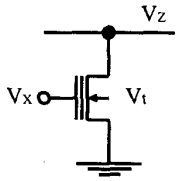


Figure 3. Multiple-valued threshold-literal circuit.

Y, respectively, are given in R-valued logic as

$$V_x = \frac{V_{dd}}{R-1}X \tag{7}$$

$$V_t = \frac{V_{dd}}{R-1}(Y+0.5) \tag{8}$$

where V_{dd} is a power supply voltage. In 4-valued logic with $V_{dd} = 5$V, V_x and V_t given by Eqs.(7) and (8), respectively, are shown in Table 1.

3.2. LVC circuit for a 4-valued universal literal

Figure 4 shows a circuit diagram to generate 6 LVC output signals. A 4-valued input signal is decoded to 4-bit binary signals, which is used as the control signals of pass transistors whose inputs are directly connected to one of 4 different supply voltage sources. 6 kinds of LVCs are realized by programming the input signals to pass transistors. The circuit configuration of the decoder is shown in Fig.5.

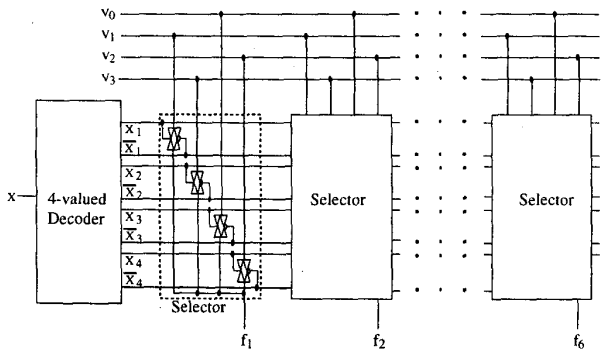


Figure 4. LVC circuit.

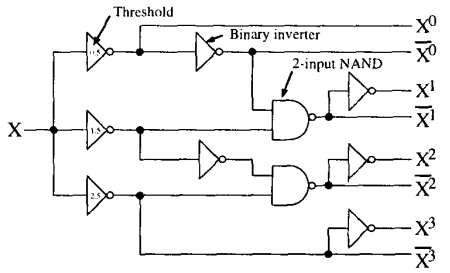


Figure 5. Circuit diagram of a 4-valued decoder.

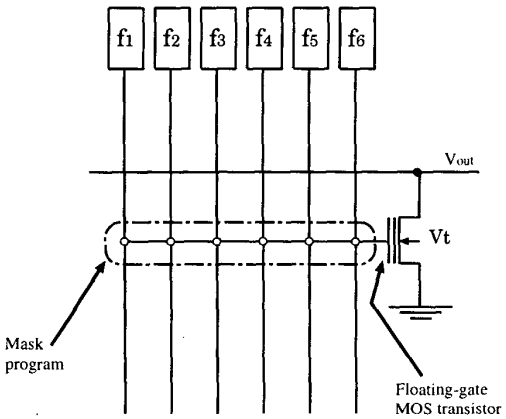


Figure 6. 4-valued universal-literal circuit.

3.3. Structure of the MIN plane

A 4-valued univeral-literal circuit is composed of a single LVC circuit and a single threshold-literal circuit as shown in Fig.6. One of 6-LVC output signals is selected as an input of a floating-gate MOS transistor by mask-programming of metal layers. At least, 6 LVCs are required to realize any 4-valued universal literal[2]. Consequently, selecting an appropriate LVC, any 4-valued universal literal can be designed by using a single 4-valued threshold-literal circuit which is realized by a single floating-gate MOS transistor. For example, the following 6 kinds of LVCs, f_1, f_2, f_3, f_4, f_5 and f_6, can be selected as

$$f_1 =< 1,3,0,2 >, f_2 =< 2,0,3,1 >, f_3 =< 0,1,2,3 >,$$
$$f_4 =< 3,2,1,0 >, f_5 =< 1,2,3,0 >, f_6 =< 2,0,1,3 > . \tag{9}$$

Figure 7 shows a circuit to realize a product of universal literals in the MIN plane. The wired-AND logic is effectively used for the MIN operation of universal literals. Each output of the MIN plane is preliminarily precharged to V_{dd}. When $X \in S$ in a universal literal X^S, an LVC cir-

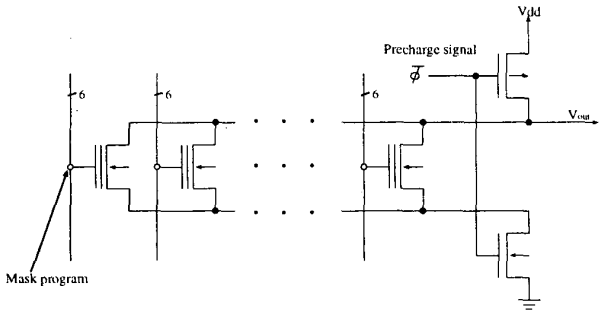


Figure 7. Realization of a product of universal literals.

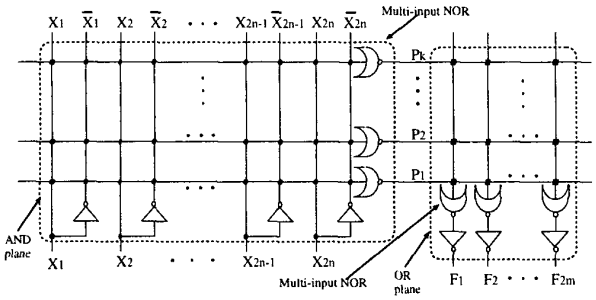
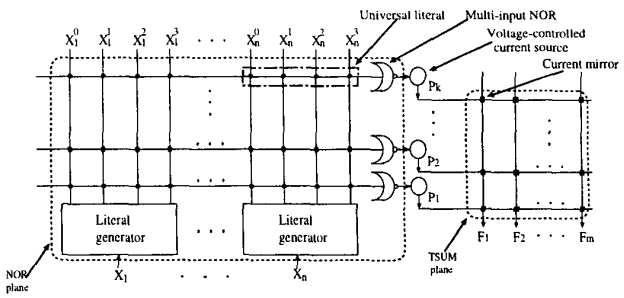
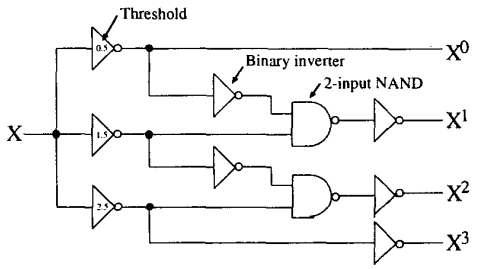


Figure 8. Structure of a binary PLA.



(a) Overall structure.



(b) Circuit diagram of a 4-valued literal generator.

Figure 9. Structure of the conventional 4-valued PLA.

cuit outputs a lower voltage than the threshold voltage of a floating-gate MOS transistor. If all universal literals satisfy $X_i \in S_i$, the output voltage V_{out} of the circuit shown in Fig.7 remains V_{dd}. Otherwise, V_{out} is pulled down to a ground level.

4. Evaluation

In order to evaluate the compactness and speed of the proposed 4-valued MPLA, we compare the performance of the proposed 4-valued PLA with that of a binary PLA [1] and a conventional 4-valued PLA [3] in this section.

4.1. Comparison of transistor counts in PLA's

Figure 8 shows a structure of a binary PLA based on AND/OR two-level synthesis. In the binary PLA, two-bit inputs are required to represent the corresponding 4-valued signal, where each bit is represented by two-rail complementary binary signals. Consequently, 4-bit lines are required to represent a single 4-valued input variable.

On the other hand, Figure 9(a) shows the overall structure of a conventional 4-valued PLA based on a NOR/TSUM synthesis [3]. Figure 9(b) shows a literal generator, in which a 4-valued input variable is decoded to 4 binary signals. Therefore, the number of transistors in the NOR plane of the conventional 4-valued PLA is the same as that in the AND plane of the binary PLA. However, the number of transistors in the TSUM plane of the conventional 4-valued PLA is reduced to half in comparison with that in the OR plane of the binary PLA because the use of 4-valued current outputs in the TSUM makes the number of output lines half.

In the proposed multiple-valued MPLA, a universal-literal circuit in the MIN plane can be implemented by using a single floating-gate MOS transistor together with using an appropriate LVC. The number of transistors in the MIN plane of the proposed 4-valued MPLA becomes one fourth in comparison with that in the NOR plane of the conventional 4-valued PLA. Table 2 summarizes the number of transistors that are required the above three kinds of PLA's.

4.2. Comparison of performances in PLA's

Figures 10 and 11 show the transient analysis of the proposed 4-valued MPLA and the conventional 4-valued PLA, respectively, by SPICE under a 0.8μm CMOS process parameter. In the SPICE simulation, a unit current I_o of a 4-valued PLA is 20μA. Since precharge-evaluate logic with a single-phase clock is used in both 4-valued PLA's,

Table 2. Comparison of transistor counts.

	Binary PLA	Conventional 4-valued PLA	Proposed 4-valued MPLA
No. of transistors (in a MIN plane)	$4 \cdot n \cdot k$	$4 \cdot n \cdot k$	$n \cdot k$
No. of transistors (in a TSUM plane)	$2 \cdot m \cdot k$	$m \cdot k$	$m \cdot k$

n: No. of 4-valued inputs, k: No. of product lines
m: No. of 4-valued outputs

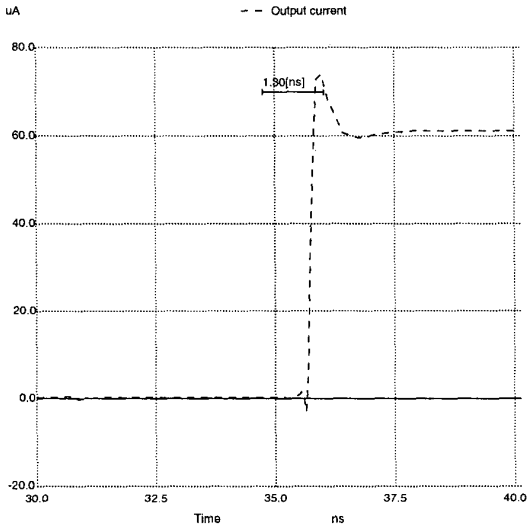


Figure 10. Transient analysis of the proposed 4-valued MPLA.

where during $\overline{\phi} = 0$ the product lines from the MIN (or NOR) plane are precharged to $V_{dd} = 5$V and the evaluation starts with the transition of $\overline{\phi}$ from low to high. The worst-case delays of the proposed 4-valued MPLA and the conventional 4-valued PLA are evaluated to be approximately 1.30 ns.

The binary PLA consists of two NOR planes and it is also designed by using precharge-evaluate logic. Two-phase clock is used to control because both product-line outputs in the NOR planes must be preliminarily precharged in a different timing, which causes a long switching delay in the binary PLA. Table 3 summarizes the comparison of the delays.

5. Conclusion

A compact multiple-valued MPLA based on a MIN/TSUM synthesis has been presented. In the MIN plane of the proposed multiple-valued MPLA, a universal literal is effectively realized by a combination of an LVC and a floating-gate MOS transistor which threshold voltage is programmable. In the 4-valued MPLA, one of 6 LVCs is selected by mask-programming an input line of a floating-gate MOS transistor. The use of mask-programming the LVC selection and programming the threshold voltage of the floating-gate MOS transistor makes the proposed MPLA compact. In fact, the transistor counts of the proposed 4-valued MPLA are the smallest of those of the other PLA's. Moreover, the switching speed of the proposed 4-valued MPLA is comparable with those of the conventional multiple-valued PLA and the binary PLA.

As a future subject, it is important to evaluate the usefulness of the proposed multiple-valued MPLA in the realization of several concrete multiple-valued logic functions.

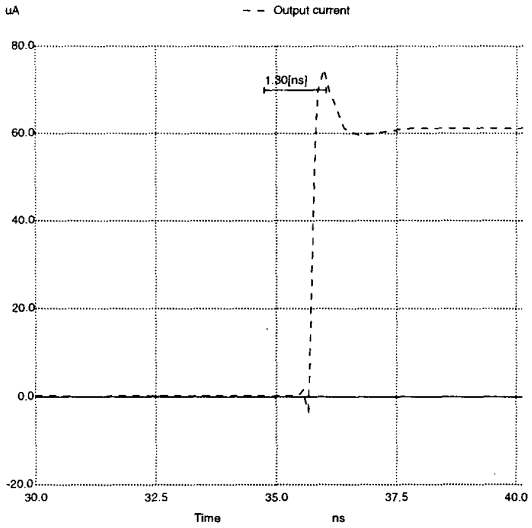


Figure 11. Transient analysis of the conventional 4-valued PLA.

Table 3. Comparison of the worst-case delays.

	Binary PLA	Conventional 4-valued PLA	Proposed 4-valued MPLA
Delay [ns]	1.06	1.30	1.30

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